# Pothukuchi, Raghavendra Pradyumna

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## AREAS OF INTEREST

Computer Architecture, Low Power High Performance systems, parallel systems, heterogeneous architectures, adaptive architectures

## EDUCATION

Aug'12-Curr. **UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN (UIUC)** GPA (curr.): 3.94/4.00
*Second year PhD student in Computer Science (CS)*

- Research Assistant with **Prof. Josep Torrellas** in the i-acoma group, Dept. of CS, UIUC

July 2011 **BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE (BITS), PILANI, INDIA** CGPA: 10.00/10.00
*B.E. (Honors) Electrical and Electronics Engineering (EEE)*

- **University Gold Medalist** for overall Academic Excellence, amongst 800 students
- Received Prof. L. K. Maheshwari Foundation Award for the **Best Graduating Student** for outstanding research efforts and all-round development, in the graduating class of 2011

## WORK EXPERIENCE

Aug'11-Jun'12. **NVIDIA GRAPHICS PVT. LTD.** Bangalore, India
*ASIC Design Engineer*

- Developed and used an automated Static Timing Analysis framework with Perl, Tcl, Synopsys PrimeTime to close timing on USB 2.0 IO modules in the 28nm **low power mobile SoC, Tegra 4**
- Analyzed and closed timing on high-speed (3.5 GHz) GDDR5/DDR3 memory interface paths in 28nm GPGPUs used for high performance computing

Jan'11-Jun'11 **NVIDIA GRAPHICS PVT. LTD.** Bangalore, India
*Hardware Design Intern*

- Developed a framework with Perl, Tcl, and HSPICE for SPICE analyses of multi voltage high-speed GPU-Framebuffer IO paths
- Studied the GPU architecture and its Single Instruction Multiple Thread model of execution

Jun'09-Jul'09 **INDIRA GANDHI CENTRE FOR ATOMIC RESEARCH** Kalpakkam, India
*Research Intern*

- Developed a micro-meter positioner read-out using a Programmable System on Chip (PSoC) based embedded system and virtual instrumentation techniques with National Instruments LabVIEW

## PUBLICATIONS

**Pradyumna, P.R.;** Tarun, C.K.S.; Bhanot, S.; , "Remote experimentation of "No-load tests on a transformer" in electrical engineering," *Engineering Education: Innovative Practices and Future Trends (AICERA), 2012 IEEE International Conference on* , pp.1-6, 19-21 July 2012

## SKILLS

| | |
|---|---|
| Computer Languages | : SPICE (Advanced), Verilog (Intermediate), C++ (Intermediate), C (Advanced), Perl (Beginner), Tcl (Beginner), |
| Software Frameworks | : LLVM, Flex, GNU Bison, HTML, CSS, MATLAB, Simulink, LabVIEW, Tora, AutoCAD |
| EDA (CAD )Tools | : PrimeTime, ModelSIM, SoC Encounter, Virtuoso Analog Environment, RTL Compiler, Calibre (DRC/LVS/PEX), OrCAD |
| Operating Systems | : Windows, Linux |

## RELEVANT COURSE WORK

GRADUATE:
Parallel Computer Architecture, Advanced Compiler Construction, Computer System Organization, Compiler Construction, Operating System Design

UNDERGRADUATE: * indicates topper of my class in the course
Analog and Digital VLSI Design*, Digital Electronics and Computer Organization*, Microelectronic Circuits*, Electronic Devices and Integrated Circuits, Microprocessor Programming and Interfacing, Communication Systems*, Image Processing*, Data Communication and Networks*, Circuits and Signals*

## COURSE PROJECTS

GRADUATE:

**Implementing a Parallel Stage Decoupled Software Pipelining (PS-DSWP) Pass in LLVM**
*(Group of 2) Guided by Prof. Vikram Adve (Dept. of CS, UIUC) as a part of Advanced Compiler Construction*
- Studied, implemented and tested this auto-parallelization pass in the LLVM Compiler framework

**Comparative Study of Traffic in a Multicore Network-on-Chip for Various Network Design Choices**
*(Group of 3) Guided by Prof. Josep Torrellas (Dept. of CS, UIUC) as a part of Parallel Computer Architectures*
- Analyzed the behavior of applications to find Network-on-Chip configurations for different power-performance tradeoffs

**A primer on Android Energy Management**
*(Group of 2) Guided by Prof. Tarek Abdelzaher (Dept. of CS, UIUC) as a part of Operating System Design*
- Studied and presented the Android Energy Management framework, identifying its strengths, weaknesses and future opportunities in gaining power efficiency

**Developing a Chaitin-Briggs Register Allocator for the LLVM Static Compiler (llc) Backend**
*(Group of 2) Guided by Prof. Vikram Adve as a part of Compiler Construction*
- Developed a Register Allocator based on Graph coloring using the LLVM Compiler Infrastructure for code generation targeting the MIPS architecture

**A study of the upcoming Intel Haswell Processor Architecture**
*(Group of 3) Guided by Prof. Sarita Adve (Dept. of CS, UIUC) as a part of Computer System Organization*
- Studied and presented the microarchitecture of the Haswell Processor

UNDERGRADUATE:

**Design of a High Speed Low power 64x64 bit Multiplier**
*(Group of 2) Guided by Prof. Anu Gupta (Dept. of EEE, BITS Pilani) as a part of Analog and Digital VLSI Design*
- Designed and implemented the full design sequence (RTL to gds extraction) of a Redundant Binary Arithmetic based 4-stage pipelined multiplier to achieve a **30% observed speedup and 40% power reduction** at 180 μm technology using Verilog and EDA Tools.

**Design of a RAM Tester**
*(Group of 3) Guided by Prof. Sudeept Mohan (Dept. of CS, BITS Pilani) as a part of Microprocessor Programming & Interfacing*
- Designed and implemented an x86 based RAM Tester that detects stuck-at-0 and stuck-at-1 faults for 8KB memory chips

## SELECTED MAJOR PROJECTS

**Mapping brain functions to a microcontroller**
- Initiated and led an interdisciplinary project to map three functions of the human brain to a microcontroller, in collaboration with students from the Department of Biological Sciences
- Won the **GE Innovation Award 2010**, presented by the John F. Welch Technology Centre, General Electric Company

**Analytical Current Voltage Modeling for Nanocrystalline Silicon Thin Film Transistors (nSi-TFT)**
*Under the guidance of Prof. Navneet Gupta (Dept. of Electrical and Electronics Engineering), BITS Pilani*

- Developed a model for nSi-TFTs and tested it using MATLAB to correlate the developed models with the observed behavior

**Remote Laboratories**
*Under the guidance of Prof. Surekha Bhanot (Dept. of Electrical and Electronics Engineering/Instrumentation) and Prof. Rahul Banerjee (Dept. of Computer Science), BITS Pilani*

- A BITS Pilani project built atop the Massachusetts Institute of Technology's iLabs shared architecture in collaboration with **MIT's Center for Educational Computing Initiatives** to enable remote experimentation using virtual laboratories
- Designed and developed a scalable embedded systems controller using LabVIEW and PSoC to automate Electrical systems experiments for the BITS-iLabs architecture

**Intelligent Power monitor and regulator**

- Designed a neural network based embedded system for efficient domestic power monitoring and regulation using MATLAB and a Programmable System on Chip
- Won the Energos challenge at APOGEE'10 [ISO 9001:2008], the International Technological Festival of BITS Pilani

## TEACHING EXPERIENCE

Aug'10-Dec'10 **MICROELECTRONIC CIRCUITS** BITS, Pilani, India
*With Prof. Anu Gupta, Dept. of Electrical & Electronics Engineering*

- Organized classroom and laboratory tutorial and teaching sessions on Microelectronics topics, Cadence Virtuoso and Eldospice tools

Aug'08-Dec'08 **ENGINEERING GRAPHICS** BITS, Pilani, India
*With Dr. Sanghamitra Kundu, Dept. of Civil Engineering*

- Assisted with organizing and developing the laboratory teaching modules using AutoCAD

## EXTRACURRICULAR ACTIVITIES & HOBBIES

Aug'09-Aug'10 **Project Coordinator** for the Electrical and Electronics Engineering Association.
Lead 4 projects and mentored 9 projects, of which 5 projects won the gold medal in respective categories at APOGEE'10, BITS Pilani

Aug'09-Aug'10 **Treasurer** of **Andhra Samiti**, a regional association consisting of students from Andhra Pradesh

Aug'08-Aug'09 **Elected member** of the **BITS Pilani Students Union**, the governing body that manages student activities of the 3000+ student body of the campus.

Jan'09-May'09 Professional Assistant in the Publication and Media Relations Unit, BITS Pilani

**Hobbies:**

- Favorite pastimes include reading historic fiction and cooking
- Writing short stories, poems in English and Telugu, my native language
- Occasionally indulge in painting, Chess and Caroms.