Pothukuchi, Raghavendra Pradyumna

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AREAS OF INTEREST

Computer Architecture, Low Power High Performance systems, parallel systems, heterogeneous architectures, adaptive architectures

EDUCATION

Aug'12-Curr. **UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN (UIUC)** GPA (curr.) : 3.94/4.00
Second year PhD student in Computer Science (CS)

- Research Assistant with **Prof. Josep Torrellas** in the i-acoma group, Dept. of CS, UIUC

July 2011 **BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE (BITS), PILANI, INDIA** CGPA: 10.00/10.00
B.E. (Hons.) Electrical and Electronics Engineering (EEE)

- **University Gold Medalist** for overall Academic Excellence, amongst 800 students
- Received Prof. L. K. Maheshwari Foundation Award for the **Best Graduating Student** for outstanding research efforts and all-round development, in the graduating class of 2011

WORK EXPERIENCE

Aug'11-Jun'12. **NVIDIA GRAPHICS PVT. LTD.** Bangalore, India
ASIC Design Engineer

- Developed and used an automated Static Timing Analysis framework to close timing on USB 2.0 IO modules in the upcoming 28nm **low power mobile SoC, Tegra**
- Analyzed and closed timing on high-speed (3.5 GHz) GDDR5/DDR3 memory interface paths in 28nm GPGPUs used for high performance computing

Jan'11-Jun'11 **NVIDIA GRAPHICS PVT. LTD.** Bangalore, India
Hardware Design Intern

- Developed a framework for SPICE analyses of multi voltage high-speed GPU-Framebuffer IO paths

Jun'09-Jul'09 **INDIRA GANDHI CENTRE FOR ATOMIC RESEARCH** Kalpakkam, India
Research Intern

- Developed a micro-meter positioner read-out using a Programmable System on Chip (PSoC) based embedded system and virtual instrumentation techniques

PUBLICATIONS

Pradyumna, P.R.; Tarun, C.K.S.; Bhanot, S.;, "Remote experimentation of "No-load tests on a transformer" in electrical engineering," *Engineering Education: Innovative Practices and Future Trends (AICERA), 2012 IEEE International Conference on*, pp.1-6, 19-21 July 2012

SKILLS

Computer Languages	: SPICE (Advanced), Verilog (Advanced), C++ (Intermediate), C (Advanced), Perl (Beginner), Tcl (Beginner)
EDA (CAD)Tools	: PrimeTime, ModelSIM, SoC Encounter, Virtuoso Analog Environment, RTL Compiler, Calibre (DRC/LVS/PEX), OrCAD
Software Frameworks	: LLVM, Flex, GNU Bison, HTML, CSS, MATLAB, Simulink, LabVIEW, Tora, AutoCAD
Operating Systems	: Windows, Linux

RELEVANT COURSE WORK

GRADUATE:
Parallel Computer Architecture, Advanced Compiler Construction, Computer Organization and Design, Compiler Construction, Operating Systems

UNDERGRADUATE: * indicates topper of my class in the course
Analog and Digital VLSI Design*, Digital Electronics and Computer Organization*, Microelectronic Circuits*, Electronic Devices and Integrated Circuits, Microprocessor Programming and Interfacing, Communication Systems*, Image Processing*, Data Communication and Networks*, Circuits and Signals*

SELECTED COURSE PROJECTS

Implementing a Parallel Stage Decoupled Software Pipelining (PS-DSWP) Pass in LLVM
(Group of 2) Guided by Prof. Vikram Adve (Dept. of CS, UIUC) as a part of Advanced Compiler Construction

- Studied, implemented and tested this auto-parallelization pass in the LLVM Compiler framework

Comparative Study of Traffic in a Multicore Network-on-Chip for Various Network Design Choices
(Group of 3) Guided by Prof. Josep Torrellas (Dept. of CS, UIUC) as a part of Parallel Computer Architectures

- Analyzed the behavior of applications to find Network-on-Chip configurations for different power-performance tradeoffs

A primer on Android Energy Management
(Group of 2) Guided by Prof. Tarek Abdelzaher (Dept. of CS, UIUC) as a part of Operating System Design

- Studied and presented the Android Energy Management framework, identifying its strengths, weaknesses and future opportunities in gaining power efficiency

SELECTED MAJOR PROJECTS

Remote Laboratories
Under the guidance of Prof. Surekha Bhanot (Dept. of Electrical and Electronics Engineering/Instrumentation) and Prof. Rahul Banerjee (Dept. of Computer Science), BITS Pilani

- Designed and developed a scalable embedded systems controller using LabVIEW to automate Electrical systems experiments for remote experimentation in the BITS-iLabs architecture, in collaboration with **MIT's Center for Educational Computing Initiatives**

Mapping brain functions to a microcontroller

- Initiated and led an interdisciplinary project to map the functions of the human brain to a microcontroller, in collaboration with a team from the Department of Biological Sciences
- Won the **GE Innovation Award 2010**, presented by the John F. Welch Technology Centre, General Electric Company

Analytical Current Voltage Modeling for Nanocrystalline Silicon Thin Film Transistors (nSi-TFT)
Under the guidance of Prof. Navneet Gupta (Dept. of Electrical and Electronics Engineering), BITS Pilani

- Developed a model for nSi-TFTs and tested it using MATLAB to correlate the developed models with the observed behavior

SELECTED TEACHING ASSISTANTSHIPS

Aug'10-Dec'10 **MICROELECTRONIC CIRCUITS** BITS, Pilani, India
With Prof. Anu Gupta, Dept. of Electrical & Electronics Engineering

- Organized classroom and laboratory tutorial and teaching sessions in Microelectronics topics and using Cadence Virtuoso and Eldospice tools.

EXTRACURRICULAR ACTIVITIES

Aug'08-Aug'09 **Elected member** of the **BITS Pilani Students Union**, the governing body that manages all activities of the 3000+ student body of the campus.

Aug'09-Dec'09 Professional Assistant in the Publication and Media Relations Unit, BITS Pilani