Pothukuchi, Raghavendra Pradyumna

504 E Clark St., Apt 32, Champaign, Illinois 61820
pothuku2@illinois.edu | **http://iacoma.cs.uiuc.edu/students/pothukuchi/**
217-281-2837

AREAS OF INTEREST

Computer Architecture, Low Power High Performance systems, parallel systems, heterogeneous architectures, adaptive architectures

EDUCATION

Aug'12-Curr. **UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN (UIUC)** GPA (curr.) : 3.94/4.00
Second year PhD student in Computer Science (CS)

- Research Assistant with **Prof. Josep Torrellas** in the i-acoma group, Dept. of CS, UIUC

July 2011 **BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE (BITS), PILANI, INDIA** CGPA: 10.00/10.00
B.E. (Hons.) Electrical and Electronics Engineering (EEE)

- **University Gold Medal** and Prof. L. K. Maheshwari Foundation Award for the **Best Graduating Student** for outstanding research efforts and all-round excellence among the class.

RELEVANT COURSE WORK

* indicates graduate coursework

Parallel Computer Architecture*, Advanced Compiler Construction*, Computer System Organization*, Compiler Construction*, Operating System Design*, Analog and Digital VLSI Design, Digital Electronics and Computer Organization, Microelectronic Circuits, Electronic Devices and Integrated Circuits, Microprocessor Programming and Interfacing

WORK EXPERIENCE

Aug'11-Jun'12. **NVIDIA GRAPHICS PVT. LTD.** Bangalore, India

- Developed and used an automated framework to close timing on high-speed (3.5 GHz) GDDR5/DDR3 memory interface paths in GPGPUs and USB 2.0 IO modules in SoC, Tegra at 28nm

Jan'11-Jun'11 **NVIDIA GRAPHICS PVT. LTD.** *(Intern)* Bangalore, India

- Developed a framework for SPICE analyses of multi voltage high-speed GPU-Framebuffer IO paths

SELECTED PROJECTS

Implementing a Parallel Stage Decoupled Software Pipelining (PS-DSWP) Pass in LLVM
(Group of 2) Guided by Prof. Vikram Adve (Dept. of CS, UIUC) as a part of Advanced Compiler Construction

- Studied, implemented and tested this auto-parallelization pass in the LLVM Compiler framework

Comparative Study of Traffic in a Multicore Network-on-Chip for Various Network Design Choices
(Group of 3) Guided by Prof. Josep Torrellas (Dept. of CS, UIUC) as a part of Parallel Computer Architectures

- Analyzed applications to find Network-on-Chip configurations for different power-performance tradeoffs

PUBLICATIONS

Pradyumna, P.R.; Tarun, C.K.S.; Bhanot, S.; , "Remote experimentation of "No-load tests on a transformer" in electrical engineering," *Engineering Education: Innovative Practices and Future Trends (AICERA), 2012 IEEE International Conference on* , pp.1-6, 19-21 July 2012

SKILLS

Computer Languages	: SPICE (Advanced), Verilog (Advanced), C++ (Intermediate), C (Advanced), Perl (Beginner), Tcl (Beginner)
EDA (CAD)Tools	: PrimeTime, ModelSIM, SoC Encounter, Virtuoso Analog Environment, RTL Compiler, Calibre (DRC/LVS/PEX), OrCAD
Software Frameworks	: LLVM, HTML, CSS, MATLAB, Simulink, LabVIEW, Tora, AutoCAD
Operating Systems	: Windows, Linux

EXTRACURRICULAR ACTIVITIES

- **Elected member** of the **BITS Pilani Students Union**, the governing body that manages all activities of the 3000+ student body of the campus
- Professional Assistant in the Publication and Media Relations Unit, BITS Pilani